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(54) **PIXEL AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME**

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(57) **ABSTRACT**

A pixel includes a first transistor coupled between a first power source and a first node, the first transistor including a gate electrode coupled to a second node, an organic light emitting diode (OLED) coupled between the first node and a second power source, a second transistor for supplying a data signal to the second node in response to a scan signal, a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled to the first power source and the second node, and a fourth transistor having a source electrode and a drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

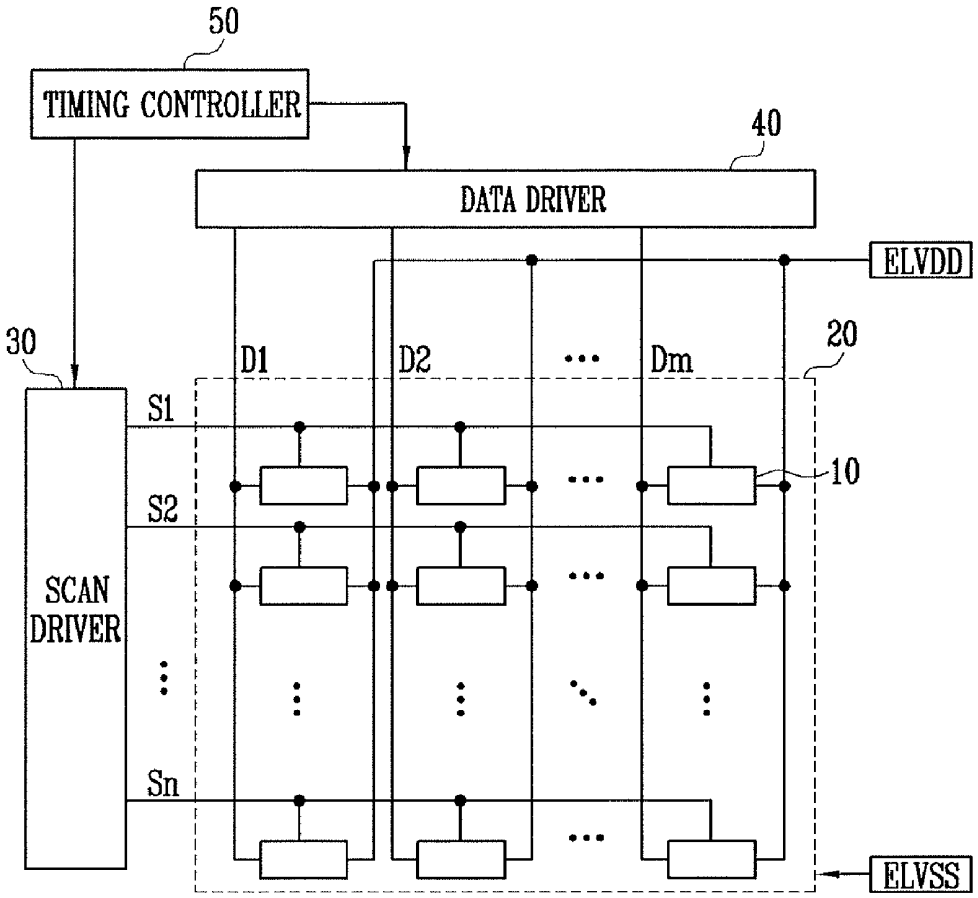


FIG. 1

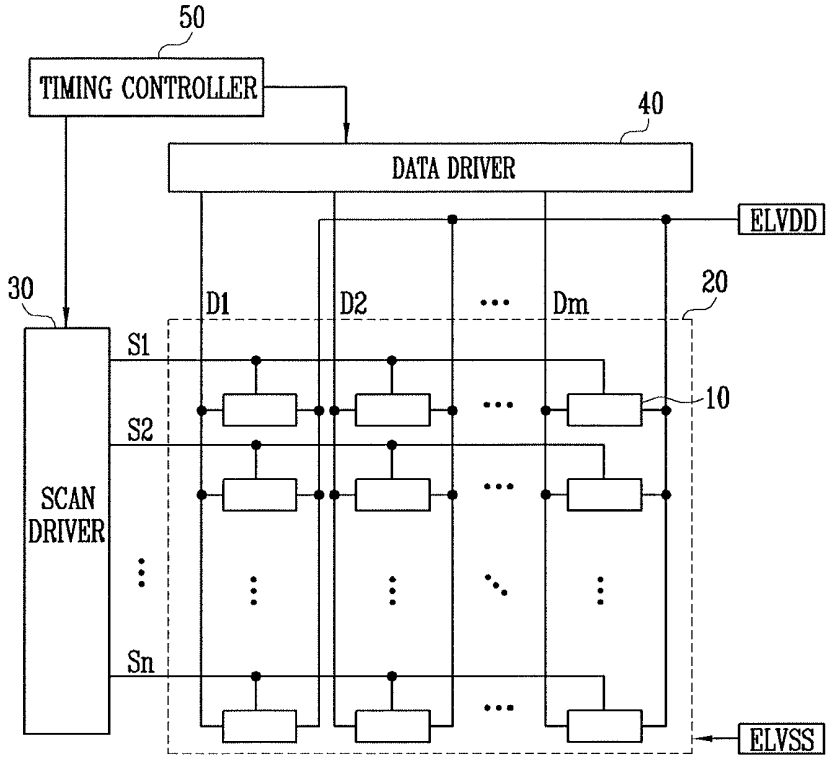

50
TIMING CONTROLLER
40
DATA DRIVER
ELVDD
30
D1
D2
Dm
20
S1
S2
10
SCAN DRIVER
Sn
ELVSS

FIG. 2

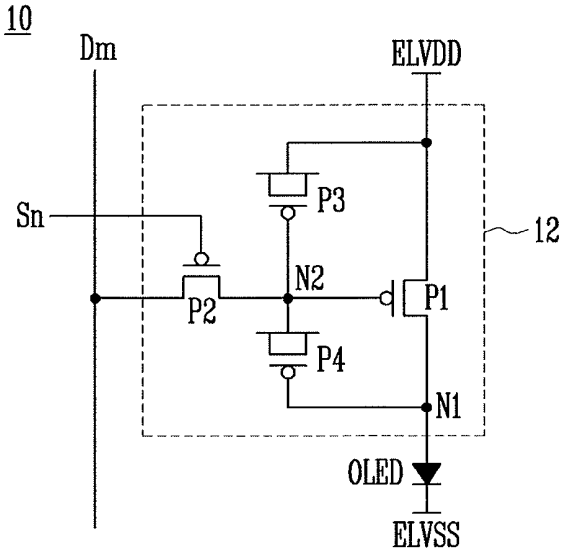

10
Dm
ELVDD
P3
Sn
12
N2
P2
P1
P4
N1
OLED
ELVSS

FIG. 3

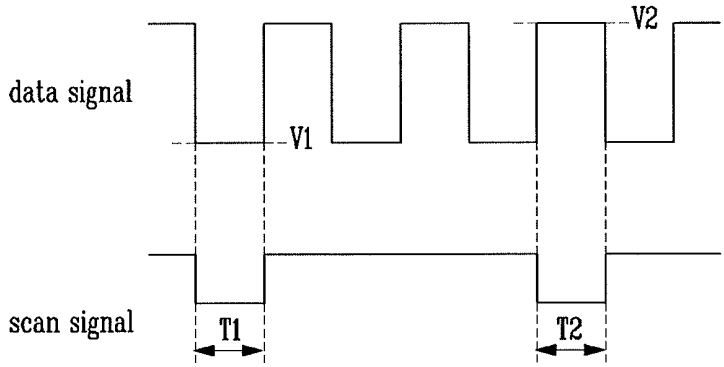

data signal
scan signal
V1
V2
T1
T2

FIG. 4

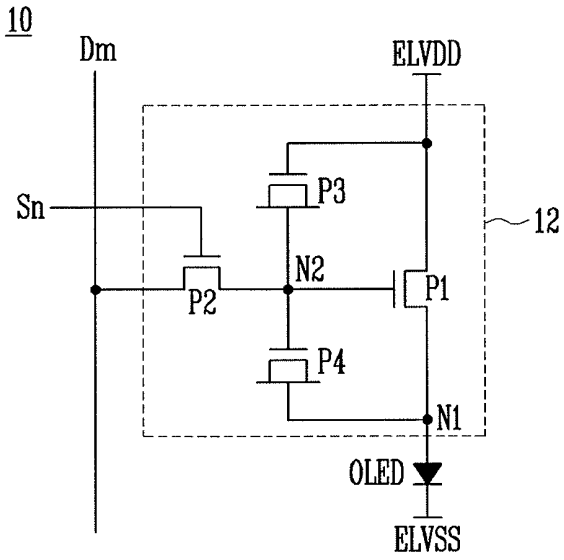

10
Dm
ELVDD
Sn
P3
12
N2
P2
P1
P4
N1
OLED
ELVSS

FIG. 5

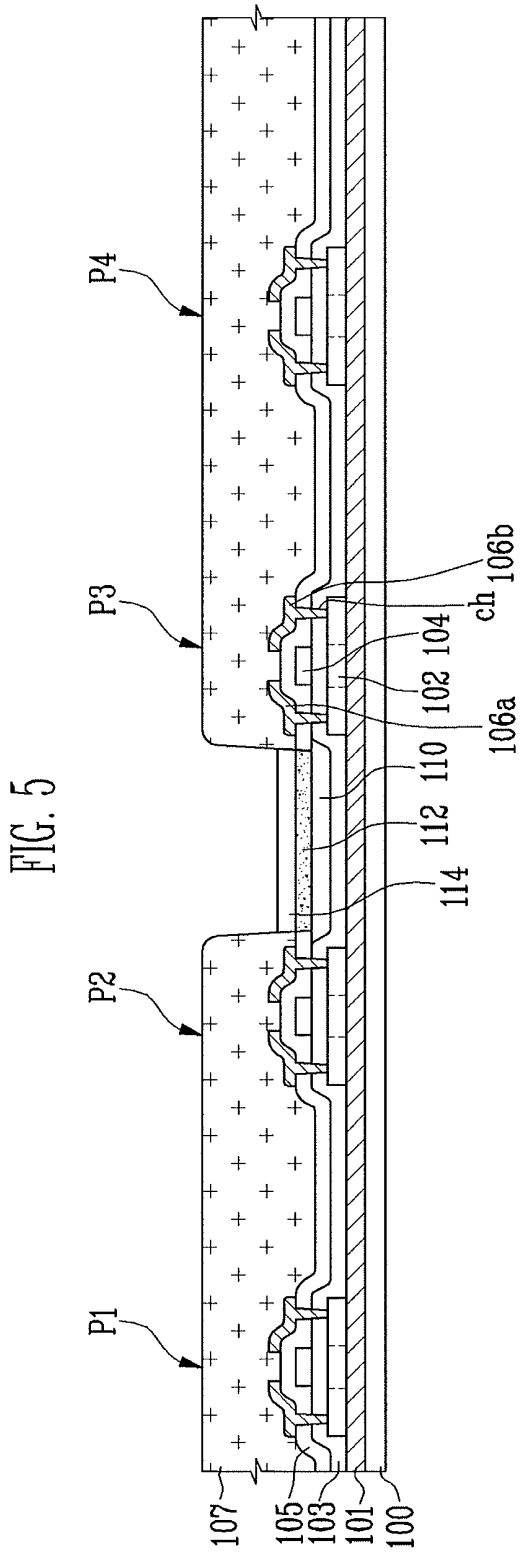


FIG. 6

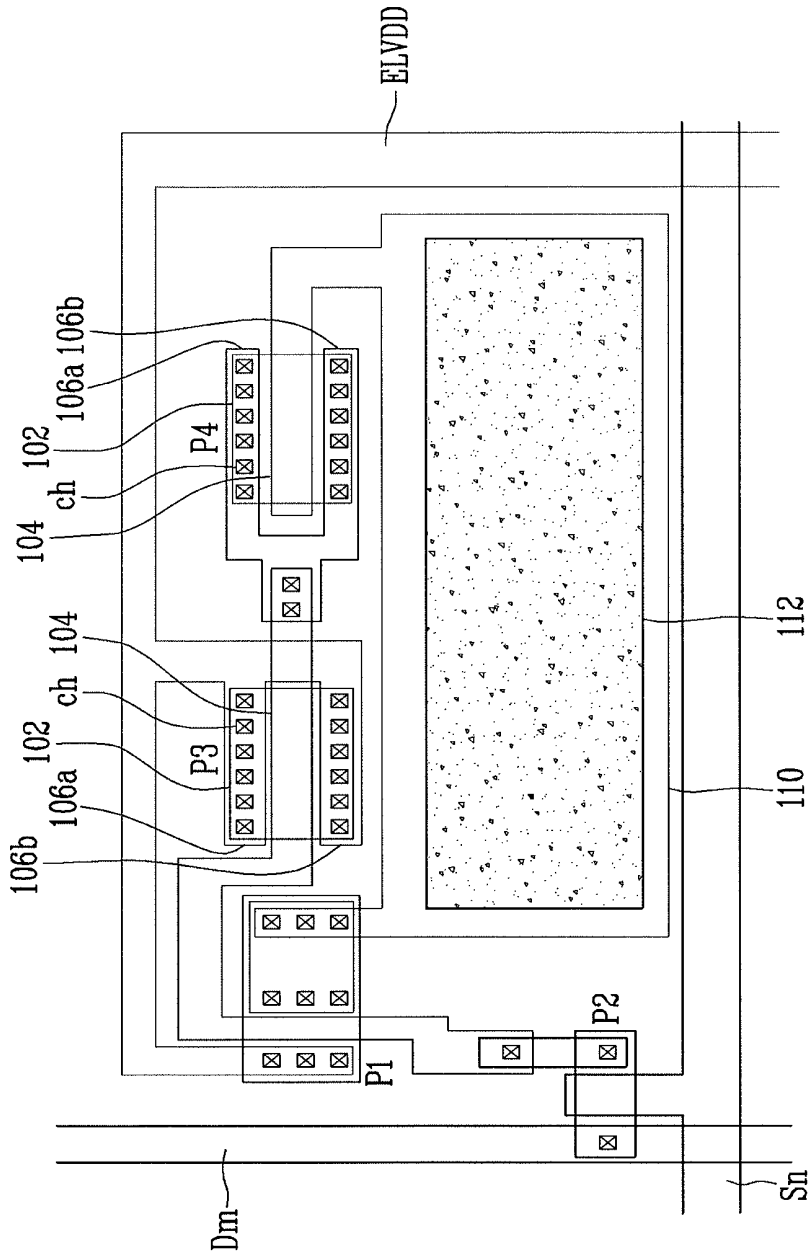

ELVDD
106b
106a
102
ch
104
P4
104
ch
102
106a
106b
P3
112
110
P2
P1
Dm
Sn

FIG. 7

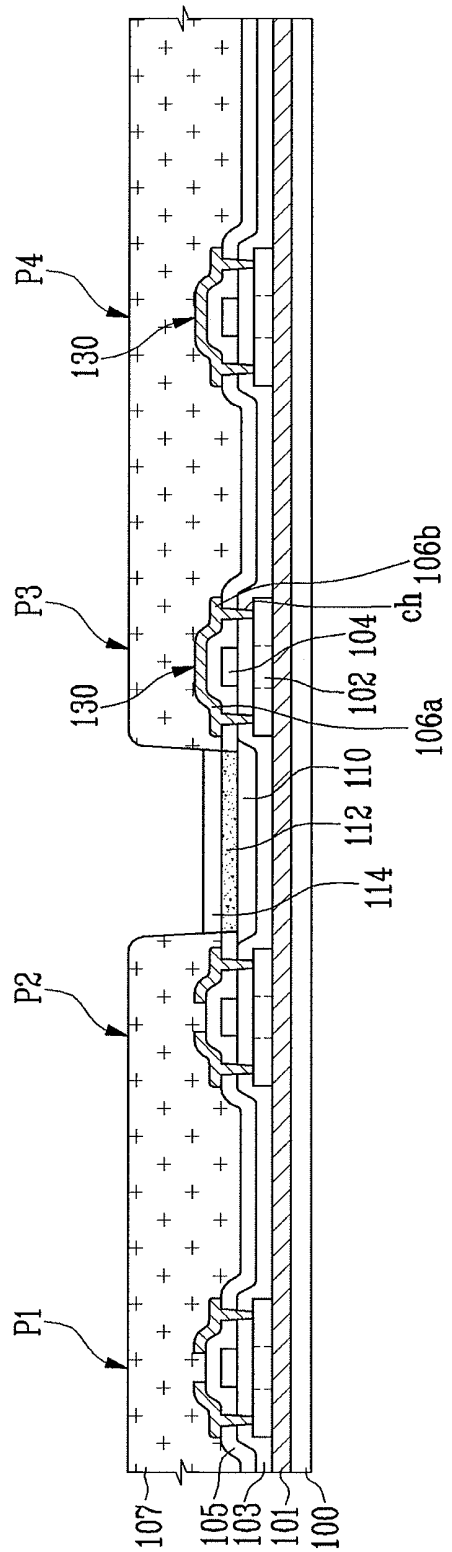

P4
130
P3
130
106b
ch
104
102
106a
110
112
114
P2
P1
107
105
103
101
100

FIG. 8

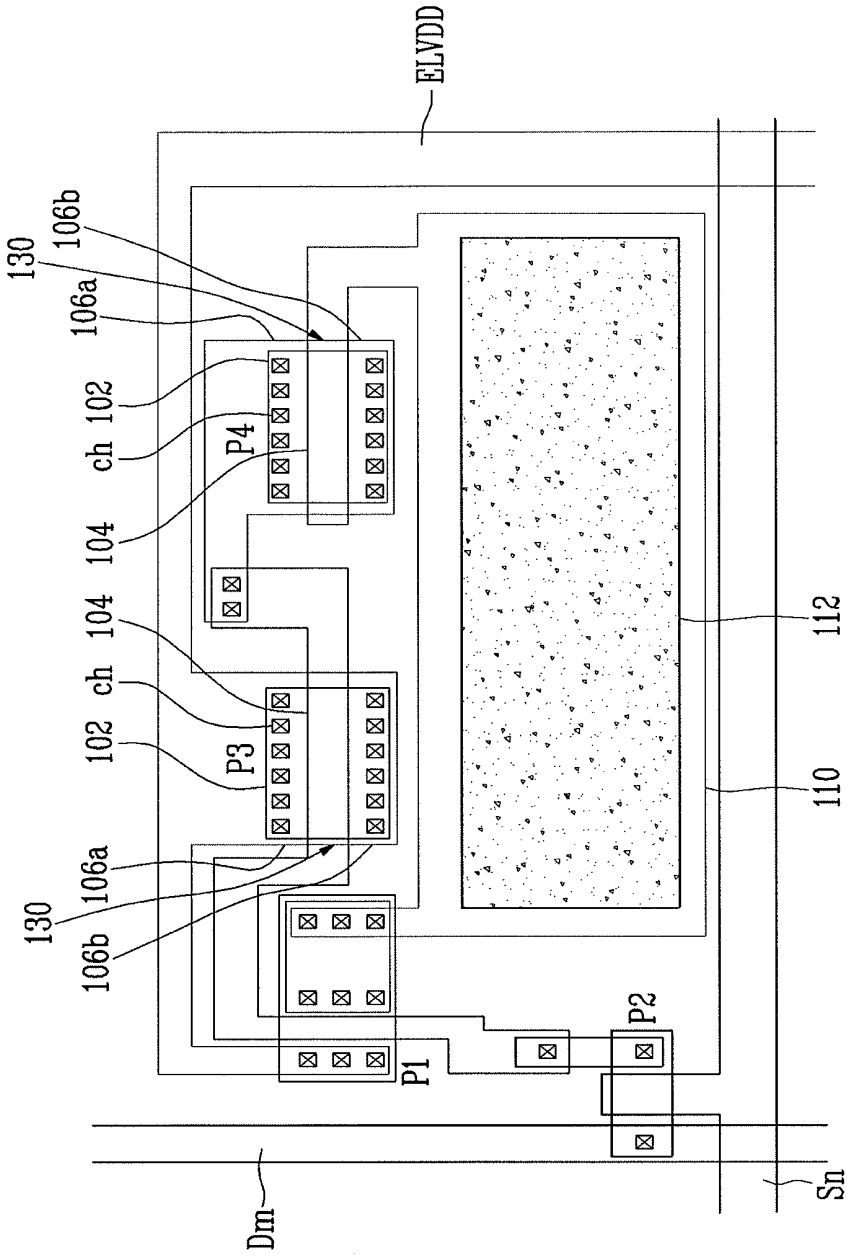
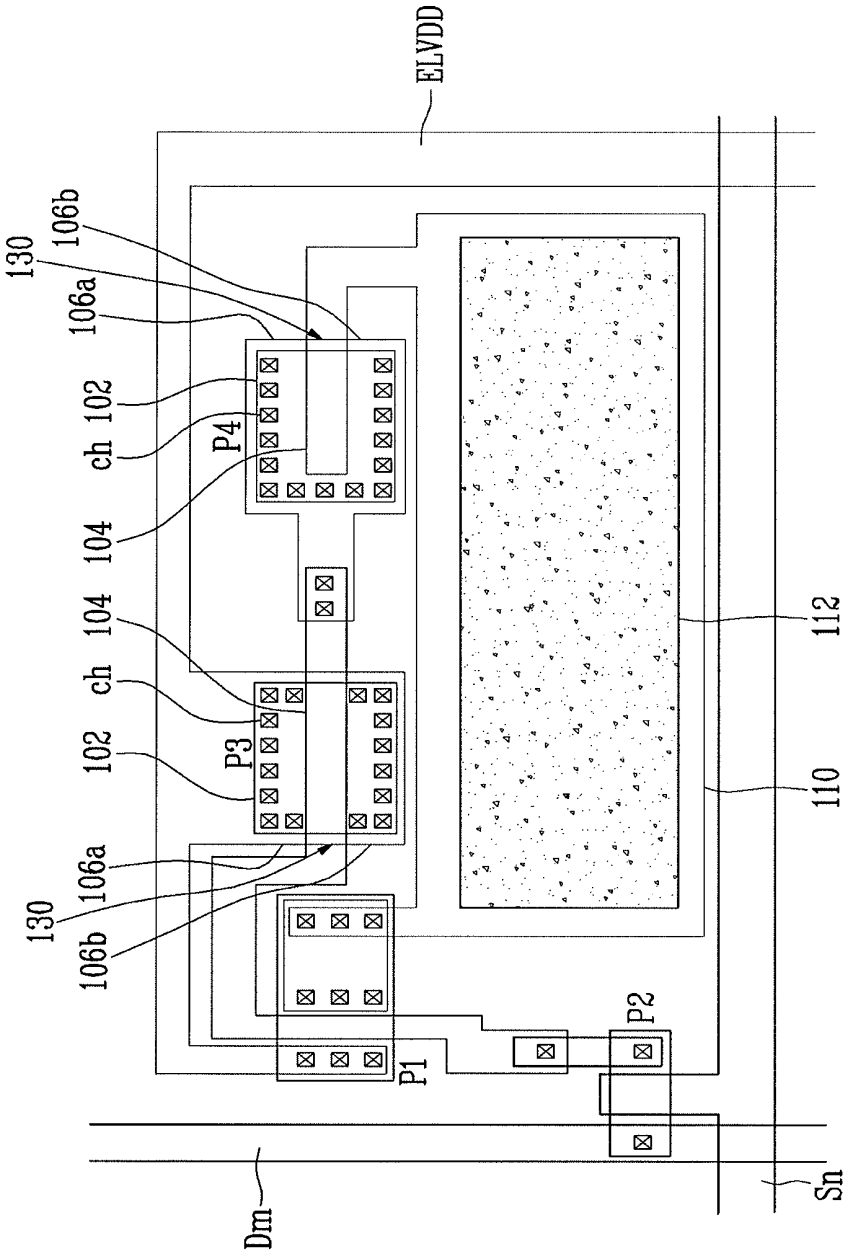

ELVDD
130
106b
106a
ch 102
104
P4
104
ch 102
P3
106a
130
106b
112
110
P2
P1
Dm
Sn

FIG. 9



PIXEL AND ORGANIC LIGHT EMITTING DISPLAY USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims priority to and the benefit of Korean Patent Application No. 10-2012-0011161, filed on Feb. 3, 2012, in the Korean Intellectual Property Office, the entire content of which is incorporated herein by reference.

BACKGROUND

[0002] 1. Field

[0003] Embodiments relate to a pixel and an organic light emitting display using the same.

[0004] 2. Description of the Related Art

[0005] Recently, various flat panel displays (FPD) capable of reducing weight and volume, which are disadvantages of cathode ray tubes (CRT), have been developed. The FPDs include liquid crystal displays (LCD), field emission displays (FED), plasma display panels (PDP), and organic light emitting displays.

[0006] Among the FPDs, the organic light emitting displays may display images using organic light emitting diodes (OLED) that generate light by the re-combination of electrons and holes. The organic light emitting display may have a high response speed and may be driven with low power consumption.

[0007] The organic light emitting display may be divided into a passive matrix type (PMOLED) and an active matrix type (AMOLED) in accordance with a method of driving the OLEDs in the display.

SUMMARY

[0008] According to an embodiment, there is provided a pixel including a first transistor coupled between a first power source and a first node, the first transistor including a gate electrode coupled to a second node, an organic light emitting diode (OLED) coupled between the first node and a second power source, a second transistor for supplying a data signal to the second node in response to a scan signal, a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled to the first power source and the second node, and a fourth transistor having another source electrode and another drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

[0009] The data signal may have a first voltage or a second voltage set to have a larger value than the first voltage.

[0010] The third transistor may be configured to operate as a MOS capacitor when a data signal having the first voltage is supplied to the second node. The fourth transistor may be configured to operate as a MOS capacitor when a data signal having the second voltage is supplied to the second node.

[0011] The third transistor may be configured to be driven in a strong inversion mode when the data signal having the first voltage is supplied to the second node. The fourth transistor is configured to be driven in a strong inversion mode when the data signal having the second voltage is supplied to the second node.

[0012] The third transistor and the fourth transistor may each include a semiconductor layer on a substrate, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer, an interlayer insulating layer on the gate electrode and the gate insulating layer. The source electrode and the drain electrode of the third transistor and the other source electrode and other drain electrode of the fourth transistor may be on the interlayer insulating layer and may be electrically coupled to the semiconductor layer through contact holes in the gate insulating layer interlayer insulating layer.

[0013] The source electrode, the drain electrode, the other source electrode and the other drain electrode may be in a form of one plate above the gate electrode. The plurality of contact holes may be formed at an edge of the plate such that a contact area between the source and drain electrodes and the semiconductor layer of the third transistor and another contact area between the other source and drain electrodes and the semiconductor layer of the fourth transistor are increased.

[0014] The first to fourth transistors may be PMOS transistors or NMOS transistors.

[0015] According to an embodiment, there is provided an organic light emitting display, including a pixel unit including pixels coupled to scan lines, data lines, a first power source, and a second power source, a scan driver for supplying scan signals to the pixels through the scan lines, and a data driver for supplying data signals to the pixels through the data lines, wherein each pixel includes an organic light emitting diode (OLED) coupled between a first node and the second power source, a first transistor coupled between the first power source and the first node, the first transistor including a gate electrode coupled to a second node, a second transistor for supplying a data signal to the second node in response to a scan signal, a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled between the first power source and the second node, and a fourth transistor having another source electrode and another drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

[0016] The data signal may have a first voltage or a second voltage, the second voltage having a larger value than the first voltage.

[0017] The third transistor may be configured to operate as a MOS capacitor when the data signal having the first voltage is supplied to the second node. The fourth transistor may be configured to operate as a MOS capacitor when the data signal having the second voltage is supplied to the second node.

[0018] The third transistor may be configured to be driven in a strong inversion mode when the data signal having the first voltage is supplied to the second node. The fourth transistor may be configured to be driven in a strong inversion mode when the data signal having the second voltage is supplied to the second node.

[0019] The third transistor and the fourth transistor may each include a semiconductor layer on a substrate, a gate insulating layer on the semiconductor layer, a gate electrode on the gate insulating layer, an interlayer insulating layer on the gate electrode and the gate insulating layer. The source electrode and the drain electrode of the third transistor and the other source electrode and other drain electrode of the fourth transistor may be on the interlayer insulating layer and may be electrically coupled to the semiconductor layer through contact holes in the gate insulating layer interlayer insulating layer.

[0020] The source electrode, the drain electrode, the other source electrode and the other drain electrode may be in a form of one plate above the gate electrode.

[0021] The plurality of contact holes may be formed at an edge of the plate such that a contact area between the source and drain electrodes and the semiconductor layer of the third transistor and another contact area between the other source and drain electrodes and the semiconductor layer of the fourth transistor may be increased.

[0022] The first to fourth transistors may be PMOS transistors or NMOS transistors.

BRIEF DESCRIPTION OF THE DRAWINGS

[0023] The accompanying drawings, together with the specification, illustrate exemplary embodiments, and, together with the description, serve to explain the principles.

[0024] FIG. **1** is a view illustrating an organic light emitting display according to an embodiment.

[0025] FIG. **2** is a view illustrating a pixel according to the embodiment.

[0026] FIG. **3** is a waveform chart illustrating a method of driving the pixel of FIG. **2**.

[0027] FIG. **4** is a view illustrating a pixel according to another embodiment.

[0028] FIG. **5** is a view illustrating the section of the pixel of FIG. **2**.

[0029] FIG. **6** is a layout diagram illustrating the pixel of FIG. **5**.

[0030] FIG. **7** is a view illustrating the section of a pixel when each of the source and drain electrodes of a third transistor and the source and drain electrodes of a fourth transistor is formed above each of the gate electrode of the third transistor and the gate electrode of the fourth transistor as one plate.

[0031] FIG. **8** is a layout diagram illustrating the pixel of FIG. **7**.

[0032] FIG. **9** is a layout diagram illustrating a pixel in which contact holes are additionally formed.

DETAILED DESCRIPTION

[0033] Korean Patent Application No. 10-2012-0011161, filed on Feb. 3, 2012, in the Korean Intellectual Property Office, and entitled: "Pixel and Organic Light Emitting Display Using the same" is incorporated by reference herein in its entirety.

[0034] Detailed items of the other embodiments are included in detailed description and drawings.

[0035] Embodiments will now be described more fully with reference to the accompanying drawings, in which exemplary embodiments of the invention are shown. However, these may be embodied in many different forms and should not be construed as being limited to the embodiments set forth herein. In the drawings, when a part is coupled to another part, the part may be directly coupled to another part and the part may be electrically coupled to another part with another element interposed. In the drawings, parts that are not related to the embodiments may be omitted for clarity of description. The same reference numerals in different drawings represent the same element, and thus their description will be omitted.

[0036] Hereinafter, a pixel according to an embodiment and an organic light emitting display using the same will be described with reference to the embodiments and the drawings for describing the embodiments.

[0037] FIG. **1** is a view illustrating an organic light emitting display according to an embodiment.

[0038] Referring to FIG. **1**, the organic light emitting display according to the embodiment includes a pixel unit **20** including pixels **10** coupled to scan lines S**1** to Sn, data lines D**1** to Dm, a first power source ELVDD, and a second power source ELVSS, a can driver **30** for supplying scan signals to the pixels **10** through the scan lines S**1** to Sn, and a data driver **40** for supplying data signals to the pixels **10** through the data lines D**1** to Dm. The organic light emitting display may further include a timing controller **50** for controlling the scan driver **30** and the data driver **40**.

[0039] Each of the pixels **10** is coupled to the first power source ELVDD and the second power source ELVSS.

[0040] Each of the pixels **10** that receive the first power source ELVDD and the second power source ELVSS generates light corresponding to a data signal by the current that flows from the first power source ELVDD to the second power source ELVSS via an organic light emitting diode (OLED).

[0041] The scan driver **30** generates the scan signals by the control of the timing controller **50** and supplies the generated scan signals to the pixels **10** through the scan lines S**1** to Sn.

[0042] The data driver **40** generates the data signals by the control of the timing controller **50** and supplies the generated data signals to the pixels **10** through the data lines D**1** to Dm.

[0043] In addition, the data driver **40** may operate so that the data signals have a first voltage V**1** or a second voltage V**2**. Here, the second voltage V**2** may be set to be larger than the first voltage V**1**.

[0044] FIG. **2** is a view illustrating a pixel according to the embodiment. In FIG. **2**, for convenience sake, the pixel **10** coupled to the nth scan line Sn and the mth data line Dm will be illustrated.

[0045] In particular, in this embodiment, transistors P**1** to P**4** that constitute the pixel **10** may be p-type metal oxide semiconductor field effect (PMOS) transistors.

[0046] Referring to FIG. **2**, each of the pixels **10** according to an embodiment includes the organic light emitting diode (OLED) and a pixel circuit **12** coupled to the data line Dm and the scan line Sn to control the amount of current supplied to the OLED.

[0047] The anode electrode of the OLED may be coupled to the pixel circuit **12** and the cathode electrode of the OLED is coupled to the second power source ELVSS. The OLED generates light of predetermined brightness to correspond to the current supplied from the pixel circuit **12**.

[0048] The pixel circuit **12** controls the current that flows from the first power source ELVDD to the second power source ELVSS via the OLED to correspond to the data signal supplied to the data line Dm when the scan signal is supplied to the scan line Sn. Therefore, the pixel circuit **12** may include a first transistor P**1**, a second transistor P**2**, a third transistor P**3**, and a fourth transistor P**4**.

[0049] The OLED is coupled between a first node N**1** and the second power source ELVSS. In detail, the anode electrode of the OLED may be coupled to the first node N**1** and the cathode electrode of the OLED may be coupled to the second power source ELVSS.

[0050] The first transistor P**1** as a driving transistor generates the current corresponding to the data signal supplied to the gate electrode of the first transistor P**1** to supply the generated current to the OLED. Therefore, the first transistor

P1 is coupled between the first power source ELVDD and the first node N1 and the gate electrode of the first transistor P1 is coupled to a second node N2.

[0051] In detail, the source electrode of the first transistor P1 may be coupled to the first power source ELVDD and the drain electrode of the first transistor P1 may be coupled to the first node N1.

[0052] The second transistor P2 may supply the data signal to the second node N2 in response to the supply of the scan signal. The second transistor P2 is turned on when the scan signal is supplied from the scan line Sn and supplies the data signal from the data line Dm to the gate electrode of the first transistor P1.

[0053] Therefore, the first transistor P1 generates the current corresponding to the voltage level of the data signal supplied to the gate electrode thereof to supply the generated current to the OLED.

[0054] In detail, the gate electrode of the second transistor P2 may be coupled to the scan line Sn, the source electrode of the second transistor P2 may be coupled to the data line Dm, and the drain electrode of the second transistor P2 may be coupled to the second node N2.

[0055] The third transistor P3 may operate as a kind of metal oxide semiconductor (MOS) capacitor. The source electrode of the third transistor P3 may be electrically coupled to the drain electrode of the third transistor P3. In detail, the source electrode and the drain electrode of the third transistor P3 may be coupled to the first power source ELVDD, and the gate electrode of the third transistor P3 may be coupled to the second node N2. Therefore, the source and drain electrodes of the third transistor P3 may be electrically coupled to each other and may be electrically coupled to the source electrode of the first transistor P1.

[0056] In particular, when a voltage (for example, the first voltage V1 of the data signal) is low enough that a channel is formed in a semiconductor layer is supplied to the gate electrode of the third transistor P3, the semiconductor layer and the gate electrode of the third transistor P3 between which a gate insulating layer is interposed may operate as one capacitor having predetermined capacitance.

[0057] The fourth transistor P4 may operate as a kind of MOS capacitor like the third transistor P3. The source electrode and the drain electrode of the fourth transistor P4 may be electrically coupled to each other. In detail, the source and drain electrodes of the fourth transistor P4 may be coupled to the second node N2, and the gate electrode of the fourth transistor P4 may be coupled to the first node N1. Therefore, the source and drain electrodes of the fourth transistor P4 may be electrically coupled to each other and may be electrically coupled to the gate electrode of the first transistor P1.

[0058] In particular, when a voltage (for example, the second voltage V2 of the data signal) is low enough that the channel is formed in the semiconductor layer is supplied to the source and drain electrodes of the fourth transistor P4, the semiconductor layer and the gate electrode of the fourth transistor P4, between which the gate insulating layer is interposed, may operate as one capacitor having predetermined capacitance.

[0059] The first node N1 may be defined as a contact point at which the anode electrode of the OLED, the drain electrode of the first transistor P1, and the gate electrode of the fourth transistor P4 are coupled to each other.

[0060] The second node N2 may be defined as a contact point at which the gate electrode of the first transistor P1, the drain electrode of the second transistor P2, the gate electrode of the third transistor P3, and the source and drain electrodes of the fourth transistor P4 are coupled to each other.

[0061] The first power source ELVDD as a high potential power source is coupled to the source electrode of the first transistor P1.

[0062] The second power source ELVSS as a low potential power source having a voltage of a lower level than the first power source ELVDD is coupled to the cathode electrode of the OLED.

[0063] FIG. 3 is a waveform chart illustrating a method of driving the pixel of FIG. 2. Hereinafter, referring to FIGS. 2 and 3, the operation of the pixel 10 according to the embodiment will be described.

[0064] First, in a first period T1, a scan signal having a voltage of a low level is supplied and a data signal having the first voltage V1 is supplied.

[0065] As the scan signal is supplied, the second transistor P2 is turned on and the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0066] The data signal supplied to the second node N2 has the first voltage V1, which is a sufficiently low voltage such that, as the first voltage V1 is supplied to the gate electrode of the third transistor P3, a channel is formed in the semiconductor layer of the third transistor P3 so that the third transistor P3 operates as a MOS capacitor.

[0067] However, as the first voltage V1 is supplied to the source and drain electrodes of the fourth transistor P4, since the channel is not formed in the semiconductor layer of the fourth transistor P4, the fourth transistor P4 does not operate as a MOS capacitor.

[0068] Therefore, a voltage corresponding to a difference between the first power source ELVDD and the first voltage V1 may be charged in the third transistor P3 that operates as a MOS capacitor so that the gate-source voltage of the first transistor P1 may be uniformly maintained until a next scan signal is supplied. Thus, the first transistor P1 generates current corresponding to the corresponding gate-source voltage so that the OLED may emit light.

[0069] Then, in a second period T2, a scan signal having a voltage of a low level is supplied and a data signal having the second voltage V2 is supplied.

[0070] As the scan signal is supplied, the second transistor P2 is turned on and the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0071] The data signal supplied to the second node N2 has the second voltage V2, which is a sufficiently high voltage such that, as the second voltage V2 is supplied to the gate electrode of the third transistor P3, the channel is not formed in the semiconductor layer of the third transistor P3, and the third transistor P3 does not operate as a MOS capacitor.

[0072] However, as the second voltage V2 is supplied to the source and drain electrodes of the fourth transistor P4, the channel is formed in the semiconductor layer of the fourth transistor P4 so that the fourth transistor P4 operates as a MOS capacitor.

[0073] Therefore, a voltage corresponding to a difference between the second voltage V2 and the voltage (the anode electrode voltage of the OLED) of the first node N1 may be charged in the fourth transistor P4 that operates as a MOS capacitor so that the first transistor P1 is turned off, until a next scan signal is supplied, to stop the emission of the OLED.

[0074] Thus, in the first period T1 where the data signal having the first voltage V1 is supplied, the third transistor P3 may operate as a MOS capacitor. However, in the second period T2 where the data signal having the second voltage V2 is supplied, the fourth transistor P4 may operate as the MOS capacitor.

[0075] In addition, when the data signal having the first voltage V1 is supplied to enhance the capacitor characteristic of the third transistor P3, the third transistor P3 may operate in a strong inversion mode. When the data signal having the second voltage V2 is supplied in order to enhance the capacitor characteristic of the fourth transistor P4, the fourth transistor P4 may operate in the strong inversion mode.

[0076] Therefore, the first voltage V1 of the data signal may be set to have a voltage value of no more than the anode electrode voltage of the OLED and the second voltage V2 of the data signal may be set to have a voltage value of no less than that of the first power source ELVDD.

[0077] FIG. **4** is a view illustrating a pixel according to another embodiment. In particular, in this embodiment, the transistors P1 to P4 that constitute the pixel **10** are n-type metal oxide semiconductor field effect (NMOS) transistors.

[0078] In this case, most of the elements of the pixel illustrated in FIG. **4** are the same as the elements of the pixel illustrated in FIG. **2**. However, the conduction type of the pixel illustrated in FIG. **4** is the reverse of the conduction type of the pixel illustrated in FIG. **2**. Accordingly, the coupling relationship between the third transistor P3 and the fourth transistor P4 is reversed.

[0079] That is, the source and drain electrodes of the third transistor P3 are coupled to the second node N2 and the gate electrode of the third transistor P3 is coupled to the first power source ELVDD.

[0080] In addition, the source and drain electrodes of the fourth transistor P4 are coupled to the first node N1 and the gate electrode of the fourth transistor P4 is coupled to the second node N2.

[0081] As a description of the operation of the pixel according to the present embodiment, in the case where the scan signal having the voltage of the high level is supplied and the data signal having the first voltage V1 is supplied, the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0082] The data signal supplied to the second node N2 has the first voltage V1, which is a sufficiently low voltage such that, as the first voltage V1 is supplied to the source and drain electrodes of the third transistor P3, a channel is formed in the semiconductor layer of the third transistor P3 so that the third transistor P3 operates as a MOS capacitor.

[0083] However, as the first voltage V1 is supplied to the gate electrode of the fourth transistor P4, since the channel is not formed in the semiconductor layer of the fourth transistor P4, the fourth transistor P4 does not operate as a MOS capacitor.

[0084] Therefore, the voltage corresponding to the difference between the first power source ELVDD and the first voltage V1 may be charged in the third transistor P3, which operates as a MOS capacitor. The gate-source voltage of the first transistor P1 may be uniformly maintained until a next scan signal is supplied. Therefore, the first transistor P1 may be turned off in a predetermined period so that the emission of the OLED may be stopped.

[0085] When a scan signal having a voltage of a high level is supplied and a data signal having the second voltage V2 is supplied, the data signal is supplied to the second node N2 by the turned-on second transistor P2.

[0086] The data signal supplied to the second node N2 has the second voltage V2, which is a sufficiently high voltage such that, as the second voltage V2 is supplied to the source and drain electrodes of the third transistor P3, the channel is not formed in the semiconductor layer of the third transistor P3, and the third transistor does not operate as a MOS capacitor.

[0087] However, as the second voltage V2 is supplied to the gate electrode of the fourth transistor P4, the channel is formed in the semiconductor layer of the fourth transistor P4 so that the fourth transistor P4 operates as a MOS capacitor.

[0088] Therefore, the voltage corresponding to the difference between the second voltage V2 and the voltage (the voltage of the anode electrode of the OLED) of the first node N1 may be charged in the fourth transistor P4, which operates as a MOS capacitor so that the first transistor P1 generates a current corresponding to the corresponding gate-source voltage until a next scan signal is supplied and that the OLED may emit light.

[0089] In addition, when the data signal having the first voltage V1 is supplied to enhance the capacitor characteristic of the third transistor P3, the third transistor P3 may operate in a strong inversion mode. When the data signal having the second voltage V2 is supplied in order to enhance the capacitor characteristic of the fourth transistor P4, the fourth transistor P4 may operate in a strong inversion mode.

[0090] FIG. **5** is a view illustrating a cross-section of the pixel of FIG. **2**. FIG. **6** is a layout diagram illustrating the pixel of FIG. **5**.

[0091] Referring to FIGS. **5** and **6**, the structures of the first to fourth transistors P1 to P4 that constitute the pixel **10** will be described in detail.

[0092] The first to fourth transistors P1 to P4 are formed on a substrate **100**. The substrate **100** may be formed of a material having an insulation property such as glass, plastic, silicon, or synthetic resin and is preferably formed of a transparent substrate such as a glass substrate.

[0093] First, the structure of the third transistor P3 will be representatively described. The third transistor P3 includes a semiconductor layer **102**, a gate insulating layer **103**, a gate electrode **104**, an interlayer insulating layer **105**, and source/drain electrodes **106***a* and **106***b*.

[0094] In addition, a buffer layer **101** may be formed on the substrate **100**. The buffer layer **101** for preventing contamination by impurities contained in the substrate **100** may be formed of an insulating material such as a silicon oxide layer SiO_2 or a silicon nitride layer SiN_X.

[0095] The semiconductor layer **102** is formed on the buffer layer **101** in a predetermined pattern. The semiconductor layer **102** may be formed of low temperature polysilicon (LTPS) obtained by crystallizing amorphous silicon deposited on the buffer layer **101** using a laser.

[0096] The gate insulating layer **103** is formed on the semiconductor layer **102**. The gate insulating layer **103** may be formed as a nitride layer or an oxide layer, for example, a silicon oxide layer or a silicon nitride layer, or other suitable materials.

[0097] The gate insulating electrode **104** is formed on the gate insulating layer **103** in a predetermined pattern. The interlayer insulating layer **105** is formed on the gate electrode **104**.

[0098] The gate insulating layer **103** insulates the semiconductor layer **102** from the gate electrode **104**. The interlayer insulating layer **105** insulates the gate electrode **104** from the source/drain electrodes **106***a* and **106***b*.

[0099] The source/drain electrodes **106***a* and **106***b* are formed on the interlayer insulating layer **105**. The source/drain electrodes **106***a* and **106***b* are electrically coupled to both sides of the semiconductor layer **102** through contact holes ch formed in the gate insulating layer **103** and the interlayer insulating layer **105**.

[0100] The gate electrode **104** and the source/drain electrodes **106***a* and **106***b* may be formed of a metal such as Mo, W, Ti, and Al or an alloy or a lamination of the above metals or other suitable materials.

[0101] A planarizing layer **107** is formed on the interlayer insulating layer **105** and the source/drain electrodes **106***a* and **106***b* and may be formed of a nitride or a oxide or other suitable materials. The anode electrode **110** of the OLED is formed in a part where the planarizing layer **107** is partially removed. The anode electrode **110** of the OLED is electrically coupled to the drain electrode of the first transistor P**1**.

[0102] In addition, a light emitting layer **112** is formed on the anode electrode **110** of the OLED. The light emitting layer **112** has a structure in which a hole transport layer, an organic light emitting layer, and an electron transport layer are laminated. A hole injection layer and an electron injection layer may be further included.

[0103] In addition, the cathode electrode **114** of the OLED is formed on the light emitting layer **112**. The cathode electrode **114** of the OLED is coupled to the second power source ELVSS.

[0104] The above-described structure of the third transistor P**3** may be applied to the remaining transistors P**1**, P**2**, and P**4**. Accordingly, a description of the structure as applied to remaining transistors P**1**, P**2**, and P**4** will not be repeated.

[0105] FIG. **7** is a view illustrating the cross-section of a pixel wherein the source and drain electrodes of a third transistor and the source and drain electrodes of a fourth transistor are each formed above the respective gate electrode of the third transistor and the gate electrode of the fourth transistor as one plate. FIG. **8** is a layout diagram illustrating the pixel of FIG. **7**.

[0106] Referring to FIGS. **5** and **6**, the source electrode **106***a* and the drain electrode **106***b* of each of the third transistor P**3** and the fourth transistor P**4** may be coupled to each other without contacting the gate electrode **104**. However, referring to FIGS. **7** and **8**, the source electrode **106***a* and the drain electrode **106***b* of each of the third transistor P**3** and the fourth transistor P**4** may be formed as one plate **130** above the gate electrode **104**.

[0107] Therefore, additional capacitance may be secured through an overlapping area formed between the plate **130** formed by the source electrode **106***a* and the drain electrode **106***b* and the gate metal **104**.

[0108] FIG. **9** is a layout diagram illustrating a pixel in which contact holes are additionally formed. Referring to FIG. **9**, a plurality of contact holes ch for coupling the source/drain electrodes **106***a* and **106***b* of the third transistor P**3** and the fourth transistor P**4** to the respective semiconductor layer **102** may be formed at the edge of the plate **130** to increase the contact area between the source/drain electrodes **106***a* and **106***b* and the semiconductor layer **102**.

[0109] As the contact area between the source/drain electrodes **106***a* and **106***b* and the semiconductor layer **102** increases, the data signal may be stably maintained.

[0110] Thus, in the third transistor P**3**, the contact holes ch may be formed at the edge on the upper and lower sides of the plate **130** formed by the source electrode **106***a* and the drain electrode **106***b*, and additional contact holes ch may be formed at the edge on the right and left sides of the plate **130**.

[0111] In addition, in the fourth transistor P**4**, additional contact holes ch may be formed at the edge only on the left side so that the contact area of the source/drain electrodes **106***a* and **106***b* and the semiconductor layer **102** may be increased.

[0112] By way of summation and review, an active matrix type organic light emitting display (AMOLED) includes a storage capacitor for charging data signals. The storage capacitor may be in the form of a metal-insulator-metal (MIM) capacitor by doping polycrystalline silicon with impurities. However, in this case, since a channel doping mask for doping semiconductor is to be added, manufacturing time and manufacturing cost are increased. In contrast, exemplary embodiments may provide a pixel of a simple structure and an organic light emitting display using the same, whereby manufacturing time and manufacturing costs may be reduced by omitting a channel doping mask.

[0113] While the embodiments been described in connection with certain exemplary embodiments, it is to be understood that the invention is not limited to the disclosed embodiments, but, on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims, and equivalents thereof.

What is claimed is:

1. A pixel, comprising:

a first transistor coupled between a first power source and a first node, the first transistor including a gate electrode coupled to a second node;

an organic light emitting diode (OLED) coupled between the first node and a second power source;

a second transistor for supplying a data signal to the second node in response to a scan signal;

a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled to the first power source and the second node; and

a fourth transistor having another source electrode and another drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

2. The pixel as claimed in claim **1**, wherein the data signal has a first voltage or a second voltage set to have a larger value than the first voltage.

3. The pixel as claimed in claim **2**, wherein:

the third transistor is configured to operate as a metal oxide semiconductor (MOS) capacitor when a data signal having the first voltage is supplied to the second node, and

the fourth transistor is configured to operate as a MOS capacitor when a data signal having the second voltage is supplied to the second node.

4. The pixel as claimed in claim **2**, wherein

the third transistor is configured to be driven in a strong inversion mode when the data signal having the first voltage is supplied to the second node, and

the fourth transistor is configured to be driven in a strong inversion mode when the data signal having the second voltage is supplied to the second node.

5. The pixel as claimed in claim **1**, wherein:

the third transistor and the fourth transistor each include:

a semiconductor layer on a substrate;

a gate insulating layer on the semiconductor layer;

a gate electrode on the gate insulating layer;

an interlayer insulating layer on the gate electrode and the gate insulating layer; and

the source electrode and the drain electrode of the third transistor and the other source electrode and other drain electrode of the fourth transistor are on the interlayer insulating layer and are electrically coupled to the semiconductor layer through contact holes in the gate insulating layer interlayer insulating layer.

6. The pixel as claimed in claim **5**, wherein the source electrode, the drain electrode, the other source electrode and the other drain electrode are in a form of one plate above the gate electrode.

7. The pixel as claimed in claim **6**, wherein the plurality of contact holes are formed at an edge of the plate such that a contact area between the source and drain electrodes and the semiconductor layer of the third transistor and another contact area between the other source and drain electrodes and the semiconductor layer of the fourth transistor are increased.

8. The pixel as claimed in claim **1**, wherein the first to fourth transistors are p-type metal oxide semiconductor (PMOS) transistors or n-type metal oxide semiconductor (NMOS) transistors.

9. An organic light emitting display, comprising:

a pixel unit including pixels coupled to scan lines, data lines, a first power source, and a second power source;

a scan driver for supplying scan signals to the pixels through the scan lines; and

a data driver for supplying data signals to the pixels through the data lines,

wherein each pixel includes:

an organic light emitting diode (OLED) coupled between a first node and the second power source;

a first transistor coupled between the first power source and the first node, the first transistor including a gate electrode coupled to a second node;

a second transistor for supplying a data signal to the second node in response to a scan signal;

a third transistor having a source electrode and a drain electrode electrically coupled to each other, the third transistor being coupled between the first power source and the second node; and

a fourth transistor having another source electrode and another drain electrode electrically coupled to each other, the fourth transistor being coupled between the second node and the first node.

10. The organic light emitting display as claimed in claim **9**, wherein the data signal has a first voltage or a second voltage set to have a larger value than the first voltage.

11. The organic light emitting display as claimed in claim **10**, wherein:

the third transistor is configured to operate as a MOS capacitor when the data signal having the first voltage is supplied to the second node, and

the fourth transistor is configured to operate as a MOS capacitor when the data signal having the second voltage is supplied to the second node.

12. The organic light emitting display as claimed in claim **10**, wherein:

the third transistor is configured to be driven in a strong inversion mode when the data signal having the first voltage is supplied to the second node, and

the fourth transistor is configured to be driven in a strong inversion mode when the data signal having the second voltage is supplied to the second node.

13. The organic light emitting display as claimed in claim **9**, wherein:

the third transistor and the fourth transistor each include:

a semiconductor layer on a substrate;

a gate insulating layer on the semiconductor layer;

a gate electrode on the gate insulating layer;

an interlayer insulating layer on the gate electrode and the gate insulating layer; and

the source electrode and the drain electrode of the third transistor and the other source electrode and other drain electrode of the fourth transistor are on the interlayer insulating layer and are electrically coupled to the semiconductor layer through contact holes in the gate insulating layer interlayer insulating layer.

14. The organic light emitting display as claimed in claim **13**, wherein the source electrode, the drain electrode, the other source electrode and the other drain electrode are in a form of one plate above the gate electrode.

15. The organic light emitting display as claimed in claim **14**, wherein the plurality of contact holes are formed at an edge of the plate such that a contact area between the source and drain electrodes and the semiconductor layer of the third transistor and another contact area between the other source and drain electrodes and the semiconductor layer of the fourth transistor are increased.

16. The organic light emitting display as claimed in claim **9**, wherein the first to fourth transistors are PMOS transistors or NMOS transistors.

* * * * *

专利名称(译)	使用其的像素和有机发光显示器		
公开(公告)号	US20130201087A1	公开(公告)日	2013-08-08
申请号	US13/467135	申请日	2012-05-09
[标]申请(专利权)人(译)	AHN JEONG瑾 李王JO		
申请(专利权)人(译)	AHN，贞瑾 李某，王某，JO		
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发明人	AHN, JEONG-KEUN LEE, WANG-JO		
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其他公开文献	US9058774		
外部链接	Espacenet USPTO		

摘要(译)

像素包括耦合在第一电源和第一节点之间的第一晶体管，第一晶体管包括耦合到第二节点的栅电极，耦合在第一节点和第二电源之间的有机发光二极管（OLED），第二晶体管，用于响应扫描信号向第二节点提供数据信号;第三晶体管，具有彼此电连接的源电极和漏电极，第三晶体管连接到第一电源和第二节点，第四晶体管具有彼此电连接的源电极和漏电极，第四晶体管连接在第二节点和第一节点之间。